OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS 2010

BSc Honours

Computer Science
CS4403 Introduction to Embedded Systems

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Answer 5 questions
(Total 80 Marks)

Time 11/2 Hours

1 (a) The low order address lines of the 8085 microprocessor are multiplexed with the data lines as AD7 – AD0 as shown in Figure 1. The '374 IC contains 8 D-type edge-triggered flip-flops as shown in Figure 2 and is used to demultiplex the address from the data lines. Explain how the demultiplexing is accomplished. (8 marks)

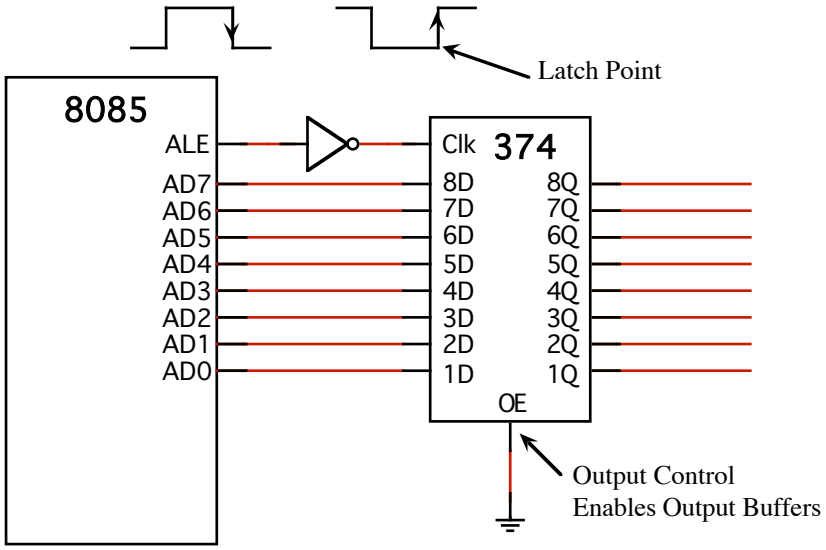

Figure 1

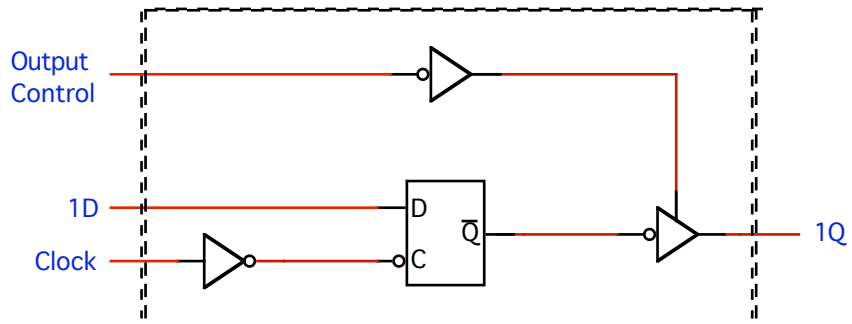

Figure 2

(b) The drive capability of an address output of the 8085 microprocessor IC is as follows: It can source 400μA at logic high and can sink 2mA at logic low. It is to be connected to ICs whose total load is I_{IH} = +2mA and I_{IL} = -18mA. The '374 IC in addition to demultiplexing is also used to provide the necessary buffering for this total load. Its DC characteristics (using the usual notation) according to the relevant data sheet are as follows:

I_{IH} = + 20μA, I_{IL} = - 400μA
I_{OL} = + 24mA, I_{OH} = - 2.6mA

Show, using a diagram, the source and sink currents at the various pins between an 8085 address output pin and a corresponding load input pin. (8 marks)

2 (a) In Figure 3 an 8-bit input device is configured for Handshake I/P at port 1. The STATUS flag is connected to bit 7 of I/P port 0. Explain, with reference to Figure 3 and the program code, the sequence of operations corresponding to reading the data. (10 marks)

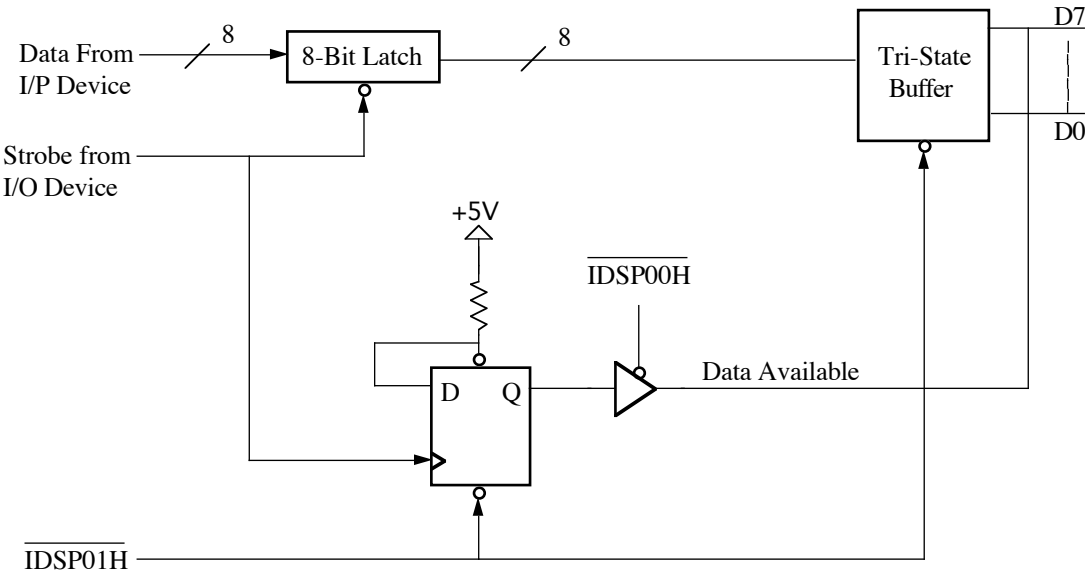

Figure 3

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INP:  IN 00H
      ANI 80H
      JZ INP
      IN 01H
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(b) Figure 4 shows how eight 8-bit input devices, each equivalent to that in part (a), might be connected to a data bus using addresses 00h through 07h. Note that a ninth input address 08h is used. Briefly explain the operation of this input system. (6 marks)

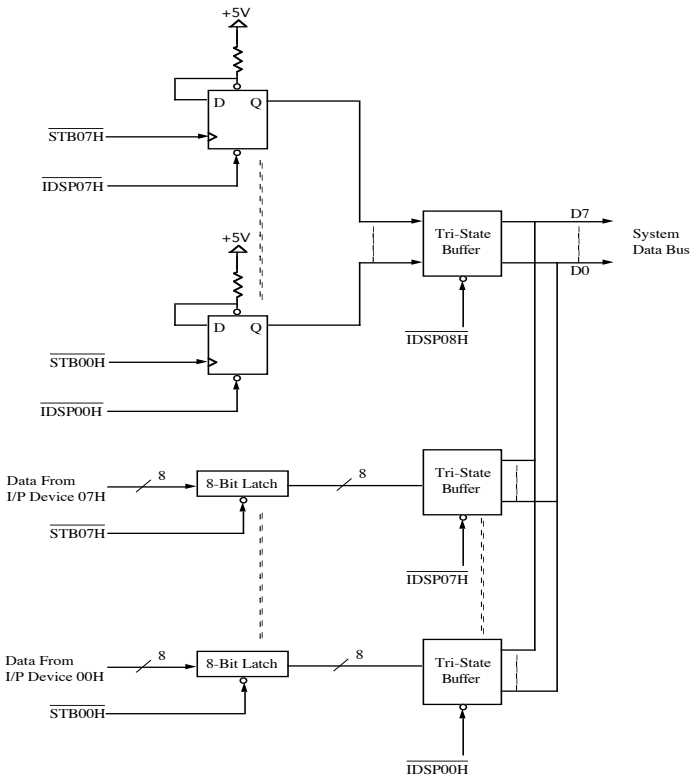

Figure 4

3 (a) Describe the 2-D address organisation used in static MOS IC memory design. Illustrate your answer using a 4Mbit ROM memory IC organised as 512Kx8. In particular, show how the logical word is extracted from the physical word. (12 marks)

(b) What differences in organization would be necessary if the IC in (a) were RW? (2 marks)

(c) What differences from the IC in (b) would be necessary if the RW IC was organized as 4Mbit x 1? (2 marks)

4 (a) Describe how the Modified Hamming code can be used to effect forward error correction. Use the following example to illustrate your answer. A 4-bit information word has single error correction and double error detection capability added using the Modified Hamming coding scheme. When the word is read the bit pattern 01001100 results. What was the original 4-bit word that was written? (6 marks)

(b) A 64Mbyte R/W memory system is constructed for use with a 32-bit processor using 4M x 1 Dram ICs. Assuming no hardware error detection capability is included, how many DRAM ICs are needed? If single error correction, double error detection (EDC) capability is added, how many extra DRAM ICs are needed? By what increments can the memory capacity be increased? (4 marks)

(c) Detail the design of the EDC part of the memory system in part (b) above. You may use a single block to depict the memory itself. Assume all memory accesses by the processor are to 32-bit words. (6 marks)

5 Figure 5 shows how up to eight devices can be connected to the vectored interrupt input on the 8085 microprocessor using the Restart instruction. Explain how it works. (16 Marks)

The RESTART instruction RST n $0 \le n \le 7$ consists of the following micro-operations:

((SP) - 1) ¬ (PCH) Load contents of PC onto the stack
((SP) - 2) ¬ (PCL)
(SP) ¬ (SP) - 2 Decrement stack pointer
(PC) ¬ 8*n Place the restart address, i.e. 8*n, in the PC

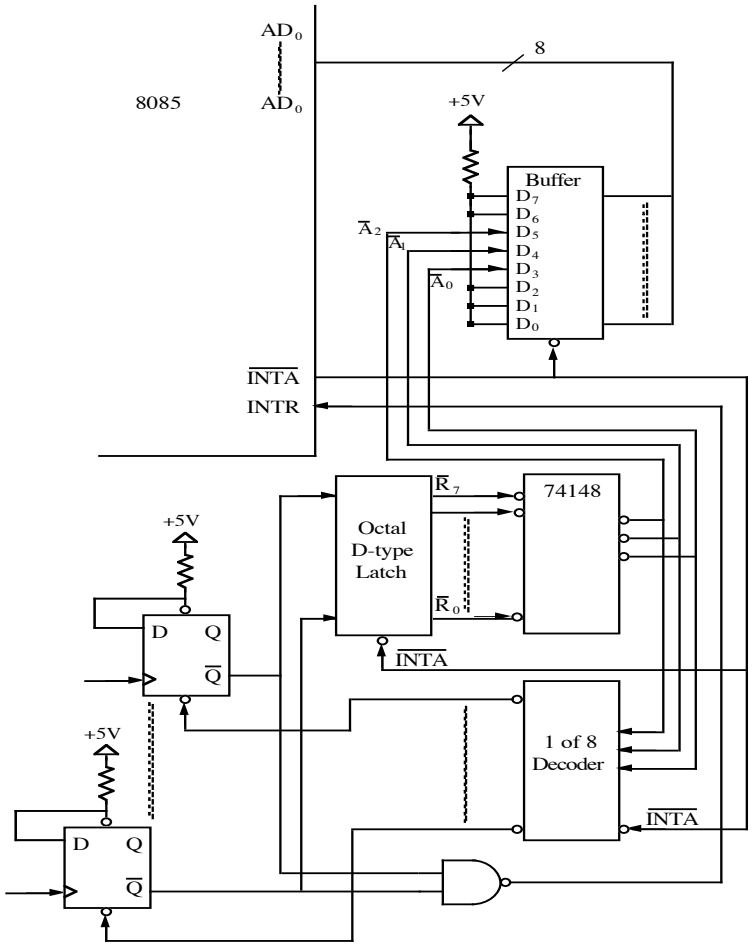

Figure 5

6 (a) In the context of asynchronous serial transmission:

(i) What functions do the start and stop bits perform and what should be their polarities? (2 marks)

(ii) Why should the receiver clock rate be a multiple of the bit rate? (2 marks)

(b) In the context of character oriented synchronous serial transmission:
What levels of synchronisation are used, what is meant by data transparency and how is it accomplished?
(6 marks)

(c) In the context of bit oriented synchronous serial transmission:
What levels of synchronisation are used, what is meant by data transparency and how is it accomplished?
(6 marks)